UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,327	03/29/2001	Toru Sasaki	PW 0245676 H7432US	2287

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EXAMINER
KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
2673	8

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☐ This action is **FINAL**.　　2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-6* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

　　If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☒ All　b)☐ Some *　c)☐ None of:

　　　1.☒ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____ .

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

　　a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

1.   This Office Action is in response to Applicant's Amendment date April 28, 2003 in

response to USPTO Office Action dated December 19, 2002.

The amendments to the specification and claims 2 and 3;   the addition of new claim 6

and Applicant's remarks have been noted and entered in the record.

Applicant's remarks relative to claim 1 are rendered moot with the introduction of new

prior art used in the rejection of claim 1.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (USP

5,473,348) taken with Kamada (USP 6,388,675) in view of Matsumoto (USP 5,929,839) and

further in view of Tanaka et al. (6,320,778).

Relative to claim 1, Fujimoto **teaches** apparatus and method of controlling paging unit of

coprocessor built in display control system (col. 2, lines 66-67;   col. 3, lines 1-67;   col. 4, lines

1-21 and col. 11, lines 12-19);   Fujimoto further **teaches** a display control apparatus comprising:

a video memory for storing color data, which are use to designate colors for displayed dots,

palette data for use in conversion of the color data and address data representing addresses of the

color data and the palette data (col. 7, lines 24-30). It being known to a person of ordinary skill

in the art at the time of the invention that the address data would have to be associated with the

color data and palette date in a video memory, in order to be able to address said data for

processing. Still further, Fujimoto **teaches** a first video memory controller for reading the palette

data from the video memory in accordance with the address data (col. 7, line 24-30);   in

addition, Fujimoto **teaches** second video memory controller (the display control system, col. 5,

lines 2-5) for reading the color data from the video memory in accordance with the address data,

so that read color data are subjected to conversion on the color palette memory in accordance

with the palette date (col. 7, lines 24-41).

Fujimoto **does not teach** a first video memory controller for reading the palette data from the

video memory in accordance with the address data so that read palette data are written to a color

palette memory;   an output circuit for outputting either the color data read from the video

memory or converted color data output from the color palette memory to a display, wherein if

present address data designating present palette data match with previous address data

designating previous palette data, the first video memory controller does not write the present

palette data to the color palette memory.

Fujimoto teaches a processing system having a central processing unit (CPU), a system memory

for storing color data, a video memory for storing an image data, and display controller means

for displaying the image data stored by the video memory on a system display.

Kamada et al. **taeches** an image processing apparatus and method (col. 2, lines 18-67;   col. 3,

lines 1-9 and Fig. 4);   Kamada et al. further **teaches** a first video memory controller for reading

the palette data from the video memory in accordance with the address data so that read palette

data are written to a color palette memory (col. 3, lines 65-67;   col. 4, lines 1-23 and Fig. 7).

It would have been obvious to a person of ordinary skill in the art to provide to the device as

taught by Fujimoto the feature as taught by Kamada et al. in order to provide an image

processing apparatus that enhance the color representation performance on one display screen

when performing coloring and displaying picture data by use of color palettes;   and further

providing an image processing apparatus that perform fast switching between color palettes (Kamada et al., col. 2, lines 18-26).

Fujimoto taken with Kamada et al. **does not teach** an output circuit for outputting either the color data read from the video memory or converted color data output from the color palette memory to a display.

Fujimoto taken with Kamada et al. teaches a processing system having a central processing unit (CPU), a system memory for storing color data, a video memory for storing an image data, and display controller means for display of the image data stored by the video memory; with the means to provide image processing that performs fast switching between color palettes.

Matsumoto **teaches** an image display control apparatus (col. 1, lines 31-67; col. 2, lines 1-67 and col. 3, lines 1-28); Matsumoto further **teaches** an output circuit for outputting either the color data read from the video memory or converted color data output from the color palette memory to a display (col. 7, lines 26-40).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Fujimoto taken with Kamada et al. the feature as taught by Matsumoto in order to put in place circuit means for generating the control and color data signal to drive the system display device.

Fujimoto taken Kamada et al. in view of Matsumoto **does not teach** the display control apparatus wherein if present address data designating present palette data match with previous address data designating previous palette data, the first video memory controller does not write the present palette data to the color palette memory.

Fujimoto taken with Kamada et al. in view of Matsumoto teaches a processing system having a central processing unit (CPU), a system memory for storing color data, a video memory for storing an image data, and display controller means for display the image data stored by the

video memory on a display; with the means to provide image processing that performs fast switching between color palettes and generates the signals to drive the system display device. Tanaka et al. **teaches** a memory device with a built-in-cache in which data can be stored for quick recall (col. 1, lines 63-67 and col. 2, lines 1-33). Tanaka et al. further **teaches** if present address data designating present palette data match with previous address data designating previous palette data, the first video memory controller does not write the present palette data to the color palette memory (col. 18, lines 9-10).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Fujimoto taken with Kamada et al. in view of Matsumoto the feature as taught by Tanaka et al. in order to include in the display control system the means to do and address compare in order to avoid writing the present palette data to the color palette memory which in turn saves the time and energy that would be expended to do the write operation.

Allowable Subject Matter

4.   Claims 2-6 are allowed.

5.   The following is an examiner's statement of reasons for allowance:

Relative to claim 2, the major difference between the teachings of the prior art of record (Fujimoto, USP 5,473,348; Matsumoto, USP 5,929,839 and Tanaka et al. 6,320,778) and that of the instant invention is that said prior art of record **does not teach** a display control apparatus wherein at completion of writing the previous palette data to the color palette memory, the first video memory controller retains the previous address data designating the previous palette data in a register, so that the first video memory controller determines whether to replace content of the color palette memory by comparison between the present address data and the previous address data.

Regarding claim 3, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a display control apparatus wherein the video memory stores a color palette replacer instruction, so that if the color pallet replacer instruction designate the color palette replacement, the first video memory controller proceeds to replacement of the content of the color palette memory unconditionally regardless of the address data.

Relative to claim 4, the major difference between the teaching of the said prior art of record and that of the instant invention is that said prior art **does not teach** a display control apparatus wherein a color palette replace signal generator for generating a color palette replacer signal based on the header data so as to make a determination whether to replace content of the color palette with respect to each of the planes, wherein if the color palette replacer instruction designates color palette replacement, the video memory controller unconditionally replaces previous palette data with present palette data on the color palette memory, while if the color palette replacer instruction does not designate color palette replacement, the video memory controller replaces the previous palette data with the present pallet data on the color palette memory only when a present color palette pointer designating the present palette data differs from a previous color-pallet pointer designating the previous palette data.

As to claim 6, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a display control apparatus

wherein if the color palette replacer instruction designates the color palette replacement, the first

video memory controller proceeds to replacement of the content of the color palette memory

unconditionally, regardless of the present or previous address data.

Conclusion

6.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

U. S. Patent No.	5,559,952	Fujimoto
U. S. Patent No.	5,500,654	Fujimoto
U. S. Patent No.	5,400,334	Hayssen

Responses

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020.

The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the

organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is 703 306-0377.

Vincent E. Kovalick
September 5, 2003

Amare Mengistu
Primary Examiner